



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/734,388	12/11/2000	John V.W. Reynders	P5431	4232

25181 7590 04/21/2004

FOLEY HOAG, LLP  
PATENT GROUP, WORLD TRADE CENTER WEST  
155 SEAPORT BLVD  
BOSTON, MA 02110

EXAMINER

KANG, INSUN

ART UNIT	PAPER NUMBER
----------	--------------

2124

DATE MAILED: 04/21/2004

9

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

**Application**

09/734,388

**Applicant(s)**

REYNDERS, JOHN V.W.

**Examiner**

Insun Kang

**Art Unit**

2124

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 1/29/2004.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-5, 8-15 and 18-24 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-5, 8-15 and 18-24 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

### DETAILED ACTION

1. This action is in response to the amendment filed 1/29/2004.
2. As per applicant's request, claims 1-3, 9, 11-13, 19 and 22-24 have been amended and claims 6, 7, 16 and 17 have been cancelled. Claims 1-5, 8-15 and 18-24 are pending in the application.

### ***Claim Rejections - 35 USC § 112***

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

4. Claims 1-5, 8-15 and 18-24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.
5. Claims 1, 11 and 22-24 recite the limitation "the minimal said execution time" in lines 28-29 (pg 2), lines 4-5 (pg 5), lines 16-17 (pg 7), lines 24-25 (pg 8) and lines 28-29 (pg 9). There is insufficient antecedent basis for this limitation in the claims. It is interpreted as "a minimal execution time."

The limitation "said expressions" in the context of "including data representing said expressions" in the claims. There is insufficient antecedent basis for this limitation in the claims. It is interpreted as "said plurality of expressions."

The limitation "the sequence in which said expressions occur" in the claims. It is unclear whether it means the sequence of expressions or the

Art Unit: 2124

execution sequence. It is interpreted as "the sequence in which said plurality of expressions are executed."

Per claims 2-5, 8-10 and 12-21, these claims are rejected for dependency on the above rejected parent claims 1 and 11.

***Claim Rejections - 35 USC § 103***

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 1-5, 8-15 and 18-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hardwick (US 6,106,575), in view of Ball (US 5,615,357), further in view of Tandri (US Patent 6,341,371).

-- In regards to claims 1, 11, and 21-24, Hardwick discloses the self-tuning vector objects for optimization on parallel computers since vectors have well-established semantics and are suitable for divide and merge operations (Hardwick, col 12 lines 14-31, col 17 lines 1-67). Hardwick discloses various automated tuning functions associated with the vector objects using optimization techniques such as divide and merge and dynamic load balancing (Hardwick, col 17 lines 1-50, col 29 lines 23-67, col 30 lines 1-52, and col 37 lines 5-50).

Hardwick discloses receiving a user program (Hardwick, col 4 lines 64-67, and col 5 lines 1-7), but doesn't explicitly teach simulating execution of said user program. Simulations are used for discovering design errors, optimizing or fine-tuning a system, evaluating system performance, or simply better understanding a complex system through analysis. Ball explicitly teaches execution-driven simulators (Ball, col 2 lines 30-60) for the purpose of accurately evaluating performance of processor designs and detecting design errors.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Ball to the method of Hardwick. The modification would be obvious because simulating the execution of a program rapidly detects potential bottlenecks and hidden problems/weaknesses in a program design so that costly delays and errors can be minimized by more accurate forecasts and estimates before actual execution.

Hardwick discloses a method comprising detecting a plurality of expressions...in said user program (Hardwick, col 3 lines 47-56, col 6 lines 41-59, col 8 lines 33-57, and col 10 lines 32-40). Hardwick discloses a trace file including data representing said expressions and indicating the sequence in which said expressions occur (Hardwick, col 6 lines 46-54 and col 32 lines 44-61) and enabling generation of source code corresponding to said expressions (Hardwick, col 8 lines 15-30).

Hardwick does not explicitly disclose dividing the trace file into blocks during simulation. Ball discloses a trace file indicating a sequence of expressions divided into a plurality of trace file blocks, so that data dependencies between

Art Unit: 2124

trace blocks are minimized, execution time is shorten, network locality is maximized, and latency is lowered due to fewer hops between processors (Ball, col 2 lines 30-60, col 3 lines 14-25, col 6 lines 30-51, col 8 lines 7-67, col 9 lines 1-65, and col 7 lines 40-54).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention was made to incorporate the teaching of Ball to the method of Hardwick. The modification would be obvious because dividing trace file into a plurality of trace file blocks can reduce data dependencies and greater network locality of processors can be achieved.

Hardwick discloses converting (Hardwick, col 8 lines 15-30), generating a plurality of minimal timing (Hardwick, col 12 lines 1-13, col 10 lines 32-54, and col 11 lines 41-55), compiled expression blocks, each of said plurality of minimal timing, compiled expression blocks corresponding to a respective one of said source code expression blocks (Hardwick, col 12 lines 5-6, 56-63, col 14 lines 52-63, cl 15 lines 10-19, col 13, col 14, and col 16 lines 1-19).

**Hardwick and Ball do not explicitly teach parameterizing the source code expression block to include at least one of a loop blocking and a loop unrolling parameter as claimed. However, Tandri discloses that a loop unrolling optimization technique was known in the art of software development, at the time applicant's invention was made, to optimize loop execution by parameterizing a source code block to include a loop unrolling parameter ("unroll factor") in col 2 lines 31-67("profiling a loop of the executing program to determine a parameter for the loop...compiling**

the program with a plurality of unroll factors prior to execution,” col 2 lines 30-67). It would have been obvious for one skilled in the art of computer software development to modify the disclosed system of Hardwick and Ball to include parameterization of source code by including a loop unroll factor as taught by Tandri. The modification would be obvious because one skilled in the art would be motivated to “generate faster executing code (col 2 lines 11-26)” by loop unrolling optimization technique, suggested by Tandri (col 2 lines 11-26 and 50-67).

Tandri further discloses the specific loop unrolling optimization technique and iteratively selecting, compiling, measuring and identifying as claimed (“multiple versions of each loop with different unroll factors,” col 8 lines 20-52)

- selecting at least one value for said respective at least one parameter (“selection of one of said unroll factors for the loop,” col 4 lines 11-16)
- compiling said parameterized source code expression block in accordance with said at least one value for said respective at least one parameter (“compiling the program with a plurality of unroll factors prior to execution,” col 3 lines 30-35)
- measuring an execution time of object code resulting from that compiling (“measuring an execution time of the loop,” col 3 lines 10-30)
- on the basis of iteratively selecting, compiling and measuring, identifying the at least one value for said respective at least one parameter that is associated with a minimal execution time for said compiled expression

**block ("in order to determine which unroll factor is best for a particular loop it is necessary to execute that loop with all the unroll factors," col 8 lines 36-52)**

Hardwick further discloses linking said plurality of minimal timing, compiled expression blocks into said user program (Hardwick, col4 lines 32-63, and col 16 lines 1-19).

-- In regard to claims 2 and 12, Hardwick inherently discloses detecting a plurality of expressions including said at least one self-tuning object in said user program is performed by program code associated with at least one overloaded operator associated with said at least one self-tuning object (Hardwick, col 6 lines 4-59). Most of the arithmetic and relational operators are overloaded to work on arrays, which perform the specified operation on the elements of the array. Some of the mathematics functions are also overloaded to take array operands. The matrix and vector are basic classes in linear algebra computation. Hardwick discloses the data type vector for implementation of the parallel model that would be associated in data parallelism that would result in successive execution of functions using the overloaded operator (Hardwick, col 12 lines 25-31) to provide an easy to use interface, reasonable time and space efficiency. See col 10 lines 41-53, col 6 lines 41-col 7 lines 2, and col 15 lines 51-57.

-- In regard to claims 3 and 13, see the rejection of claim 2 above.



--In regard to claims 4 and 14, Hardwick discloses that dividing trace file into plurality of trace file blocks is performed such that a total amount of computational dependencies and synchronization requirements within said user program, including computational dependencies and synchronization requirements between trace file blocks are minimized (Hardwick, col 5 lines 2-8, lines 39-49, col 10 lines 10-54, col 11 lines 14-18, col 25 lines 28-40 col 27 lines 2-10, and col 14 lines 27-46).

-- In regard to claims 5 and 15, Hardwick discloses C functions delimited by curly braces in a program. For example, see col 19 lines 15-35. However, Hardwick does not explicitly disclose that dividing said trace file into said plurality of trace file blocks is performed responsive to user provided delimiters included within said user program.

Ball teaches that the trace file is generated for data/execution flow analysis containing a sequence of program instructions. Ball discloses by dividing trace files into trace file blocks, more accurate performance statistics can be obtained in a relatively short time by running a relatively small portion of a program (Ball, col 8 lines 38-65) and minimize the data/execution analysis complexity.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention was made to incorporate the teaching of Ball to the method of Hardwick. The modification would be obvious because dividing trace file into a plurality of trace file blocks is performed responsive to user provided delimiters included within said user program so that the execution

flow analysis complexity can be reduced and more accurate performance statistics can be more quickly obtained.

-- In regard to claims 8 and 18, Hardwick discloses that linking of minimal timing compiled expression blocks to user program is responsive to execution of user program (Hardwick, col 16-lines 1-19, and col 4 lines 32-38).

-- In regard to claims 9 and 19, Hardwick discloses that detecting during execution of user program, plurality of expressions including at least one self-tuning object in user program (Hardwick, col 16 lines 1-19, and col 10 lines 32-40).

-- In regard to claims 10 and 20, Hardwick discloses scheduling minimal timing compiled expression blocks for execution on at least one processor of target parallel processing computer (Hardwick, col 10 lines 32-54, and col 32 lines 34-43).

### ***Response to Arguments***

8. Applicant's arguments with respect to claims 1, 11 and 22-24 have been considered, however, they are moot in view of the new ground(s) of rejection.

### ***Conclusion***

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Insun Kang whose telephone number is 703-305-6465. The examiner can normally be reached on M-F 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on 703-305-9662. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2124

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

IK  
3/24/2004



**KAKALI CHAKI**  
**SUPERVISORY PATENT EXAMINER**  
**TECHNOLOGY CENTER 2100**